WBS 6.5.1.1
Tile Main Boards
Technical Overview

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The University of Chicago

Conceptual Design Review of the High luminosity LHC Detector Upgrades
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About the Expert

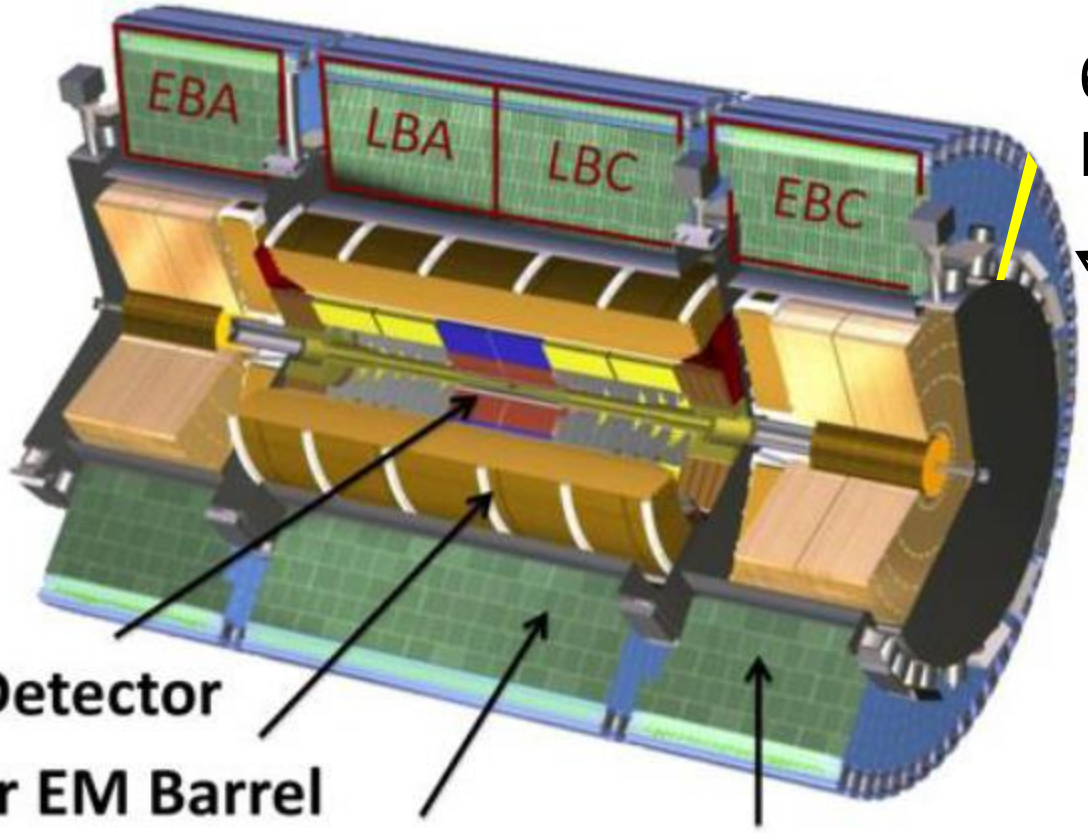
- Mark Oreglia, Professor of Physics, The University of Chicago
- Has been a member of ATLAS and the Tile Calorimeter team from the beginning (1995)
- US ATLAS Level-2 Tile Calorimeter Upgrade Construction mgr
  - Was co-leader of the CERN Tile upgrade R&D effort 2012-15
  - Was USATLAS L2 manager for TileCal upgrade R&D 2012-15
  - Authored the TileCal section of the summer 2015 upgrade scoping doc
  - Currently assisting the TileCal Project Leader in orchestrating the upgrade
- Leads the R&D effort at UChicago to design and prototype front-end boards and main control boards for the upgraded electronics; supervises two personnel in the UC Electronics Development Group:
  - Dr. Kelby Anderson, PhD, principal scientist behind the system
  - Fukun Tang, EE, principal electronics designer

About the Institution

- Large UChicago ATLAS group has been involved since day 1
  - Built 1/8 of the steel/scintillator wedges
  - Designed and built the “3in1” front-end amplifier/shaper cards
  - Designed and built the “motherboards” for the onboard electronics
  - Faculty, Postdocs, Grad students routinely in leadership roles (ops)
  - Major players in upgrade R&D
- UC is a natural candidate to produce upgrade electronics
  - Motherboard production very similar task to the upgrade main boards!
  - The same principals are designing/prototyping the upgrade
  - Strong support by University and Electronics Development Group
    - No new effort!
  - And…we already built a successful prototype!!!

The Current Tile Calorimeter

4 “barrels”, 256 modules



64 ϕ Wedges
R: 2.28-3.87m

LV “finger” boxes

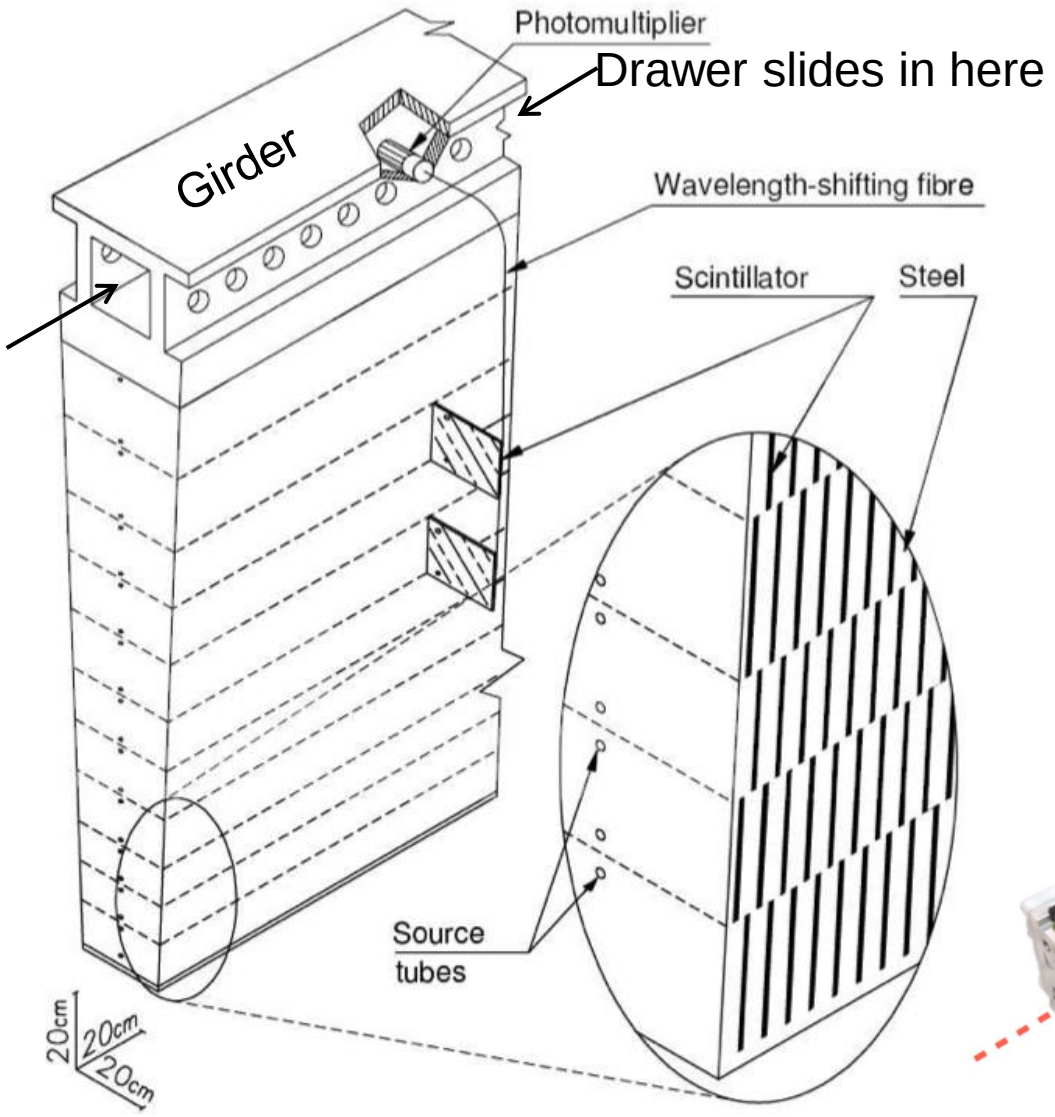
Inner Detector

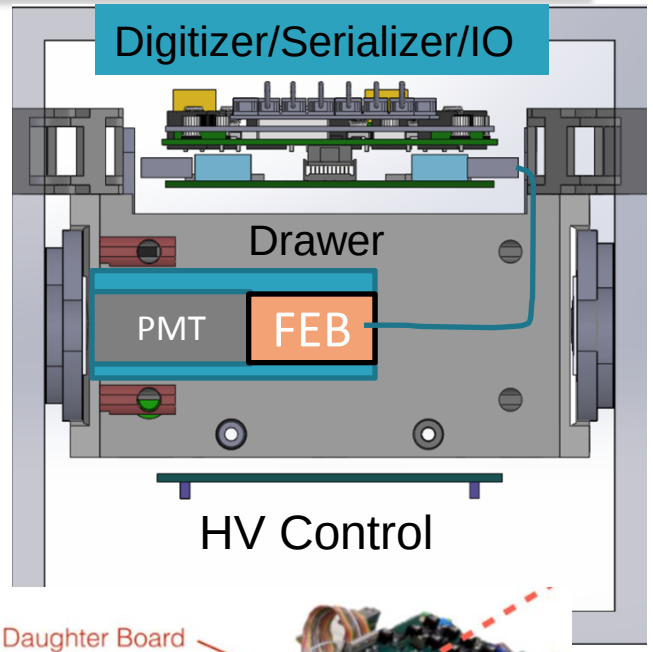
LAr EM Barrel

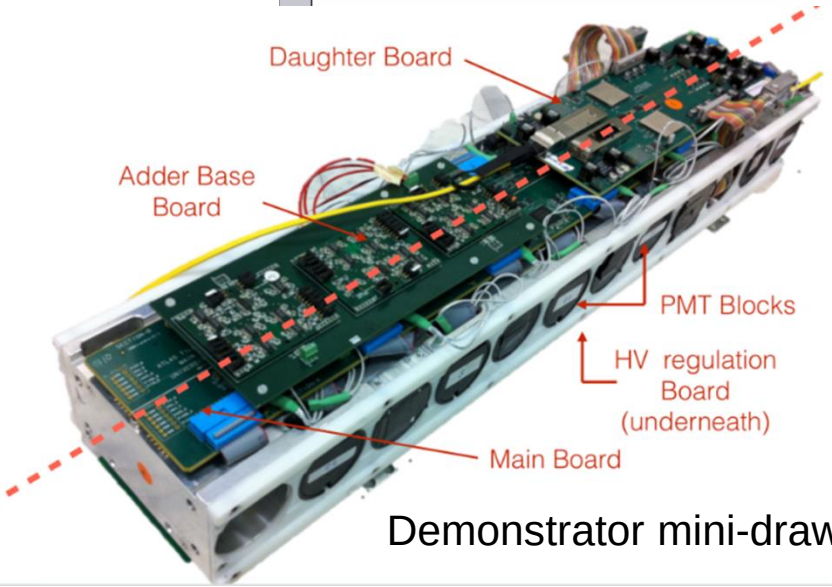
Tile Barrel

Tile Extended Barrel

Tile Wedge Structure

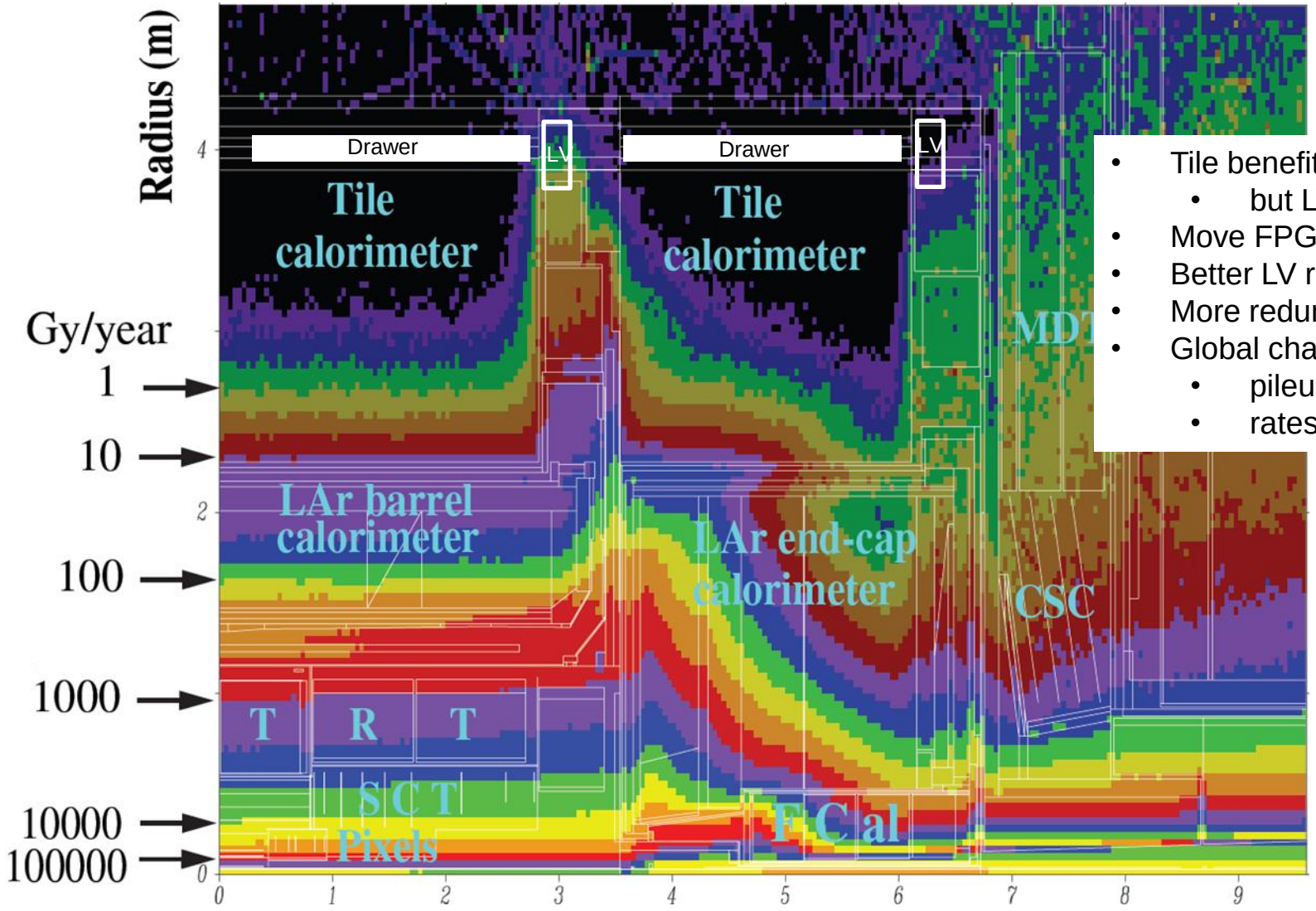






Demonstrator mini-drawer

Radiation Dose for 100 fb^{-1}



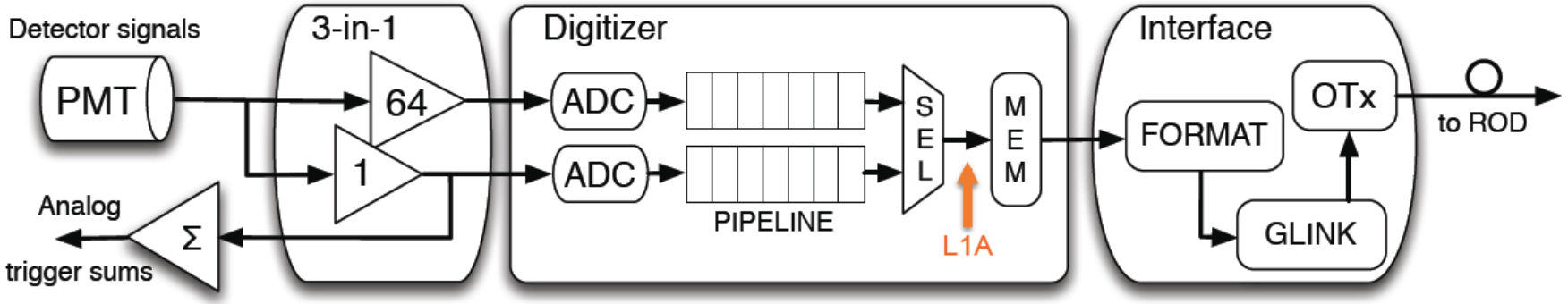
- Tile benefits from shielding
  - but LVPS in n-plume
- Move FPGAs in more
- Better LV rad tolerance
- More redundancy
- Global challenges:
  - pileup: μ=140-200
  - rates, latency

The Upgrade Strategy

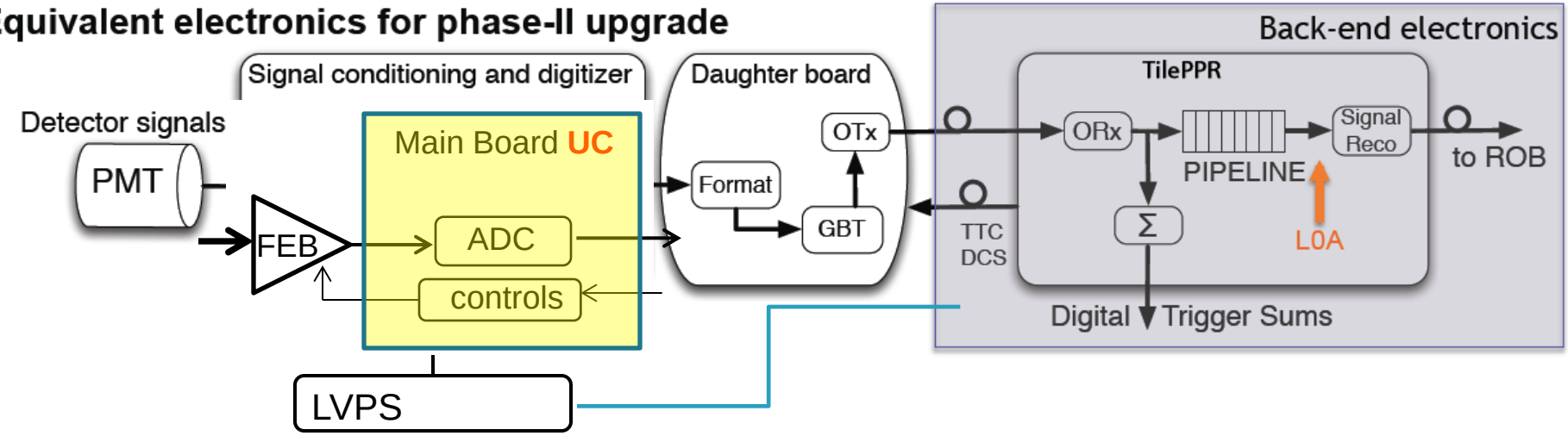
- As presented in the overview, the current electronics cannot support the trigger needed to address the physics mission
  - Data buffer too small, Tx speeds too low, analog trigger sum too noisy
- To meet the physics and trigger needs:
  - Need to buffer the data from all cells, all beam crossings off-detector
    - Flexibility in forming trigger based on energy profile over many cells
    - Ability to perform superior pileup subtraction
    - Less electronic noise means better energy resolution
- The clear solution is to **transmit the data from all calorimeter cells at the 40 MHz collision rate**; there is no cost gain by buffering or regrouping fiber

The Main Board

Present front-end electronics



Equivalent electronics for phase-II upgrade



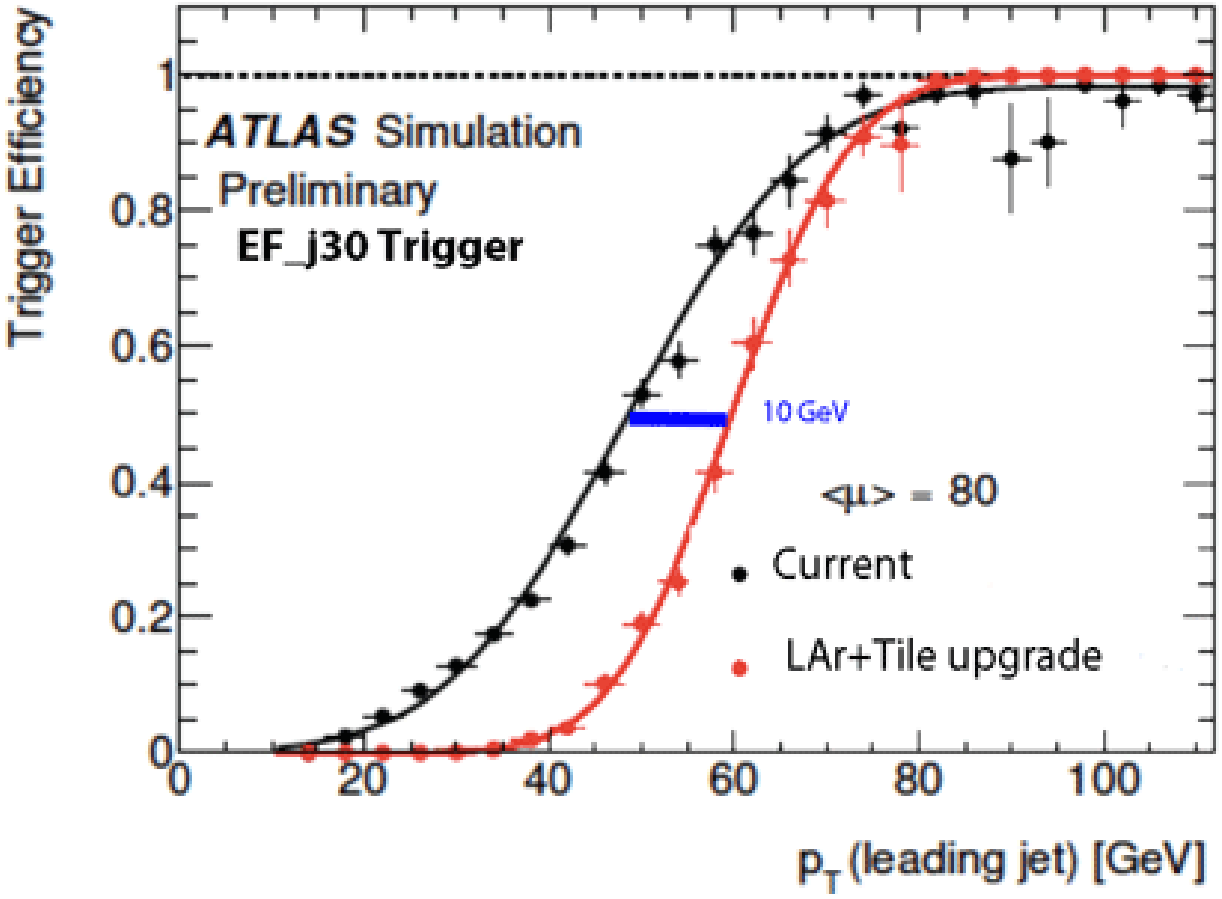
- Must digitize and transfer data from PMTs at 560 Mbps
- Electronic noise must be smaller than xxx fC
- Must generate Digital LV levels, calibration functions, control signals

Physics-driven MB Requirements

- 40 MHz trigger $\Rightarrow$ 13.44 Gbps data Tx speed
- Electronic noise < 150 fC to resolve muons
  - Muon trigger (D-cell): noise RMS < 50 fC
- Energy resolution: nonlinearity < 1 ADC count

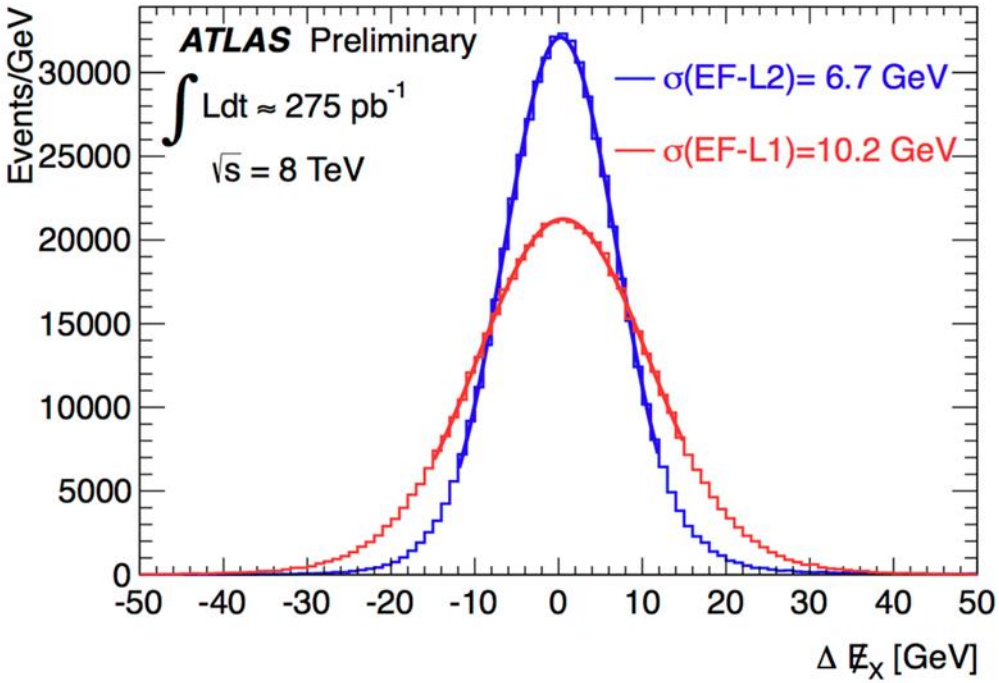
Physics Impact: Trigger

- Better energy resolution ⇒ lower trigger rate
  - below: 50% point of 30 GeV trigger raised 10 GeV ⇒x10 rate decrease



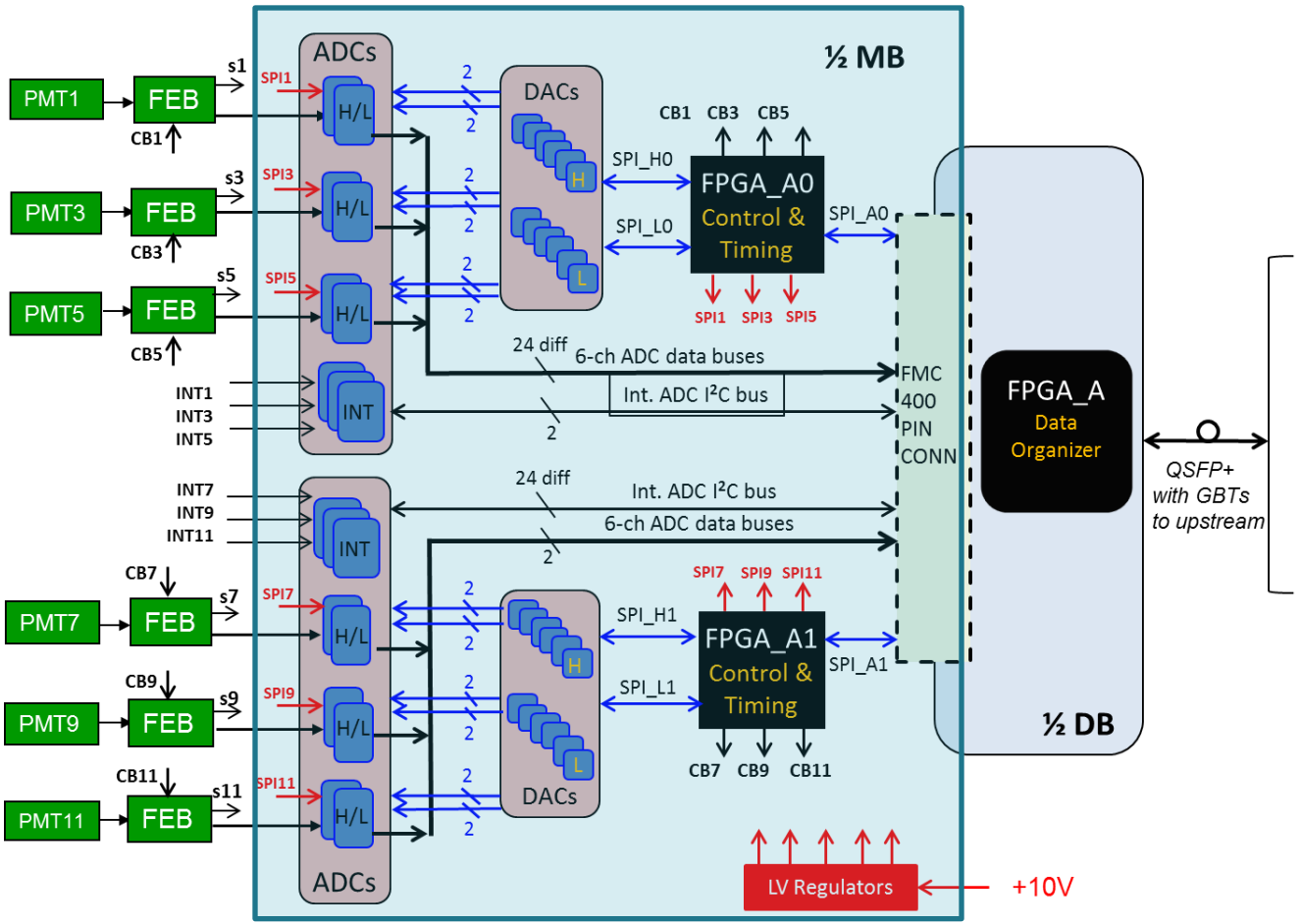
Physics Impact: Missing Energy

- Improved resolution and noise reduction vastly improves missing energy measurement
  - important for New Physics searches



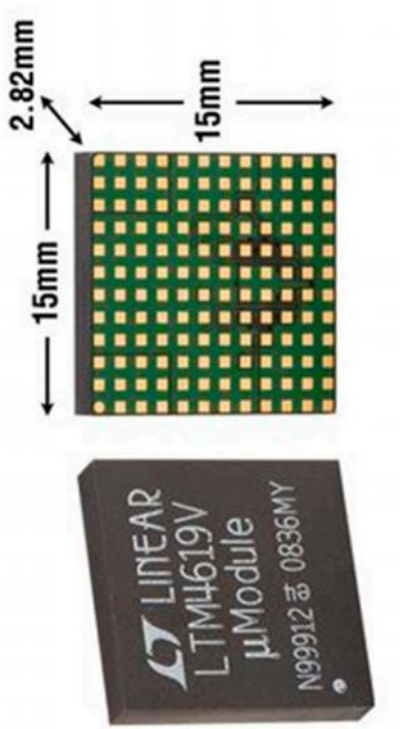
The Main Board

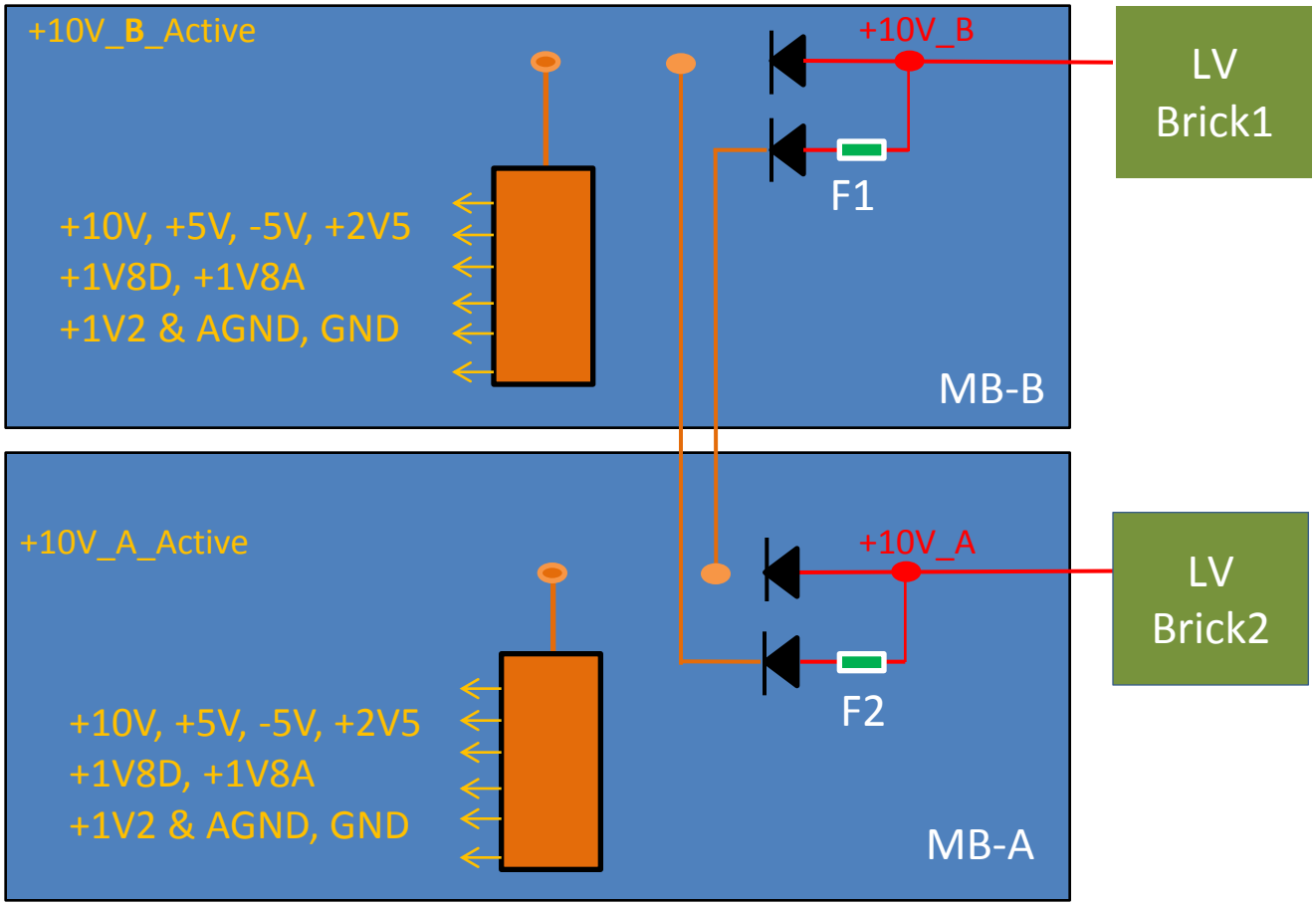
- Digitizes the PMT pulses, serializes the data, routes it to fibers
- Send control commands to the front-end cards: gains, calibrations
- Converts 10 v feed to required voltages, with redundancy



Redundant Local Power

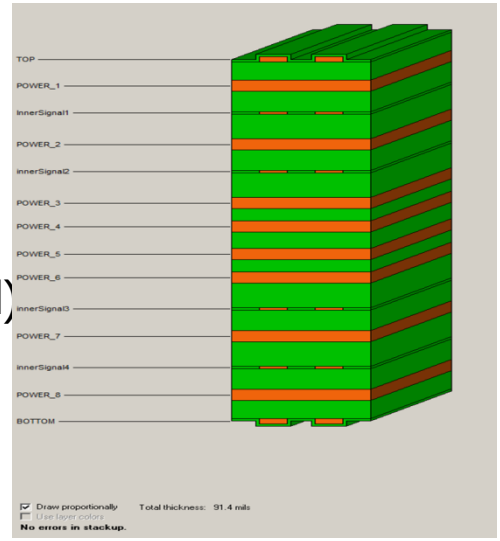
Prevent against failure from loss of LV feed
Use diode-OR and Point Of Load regulators

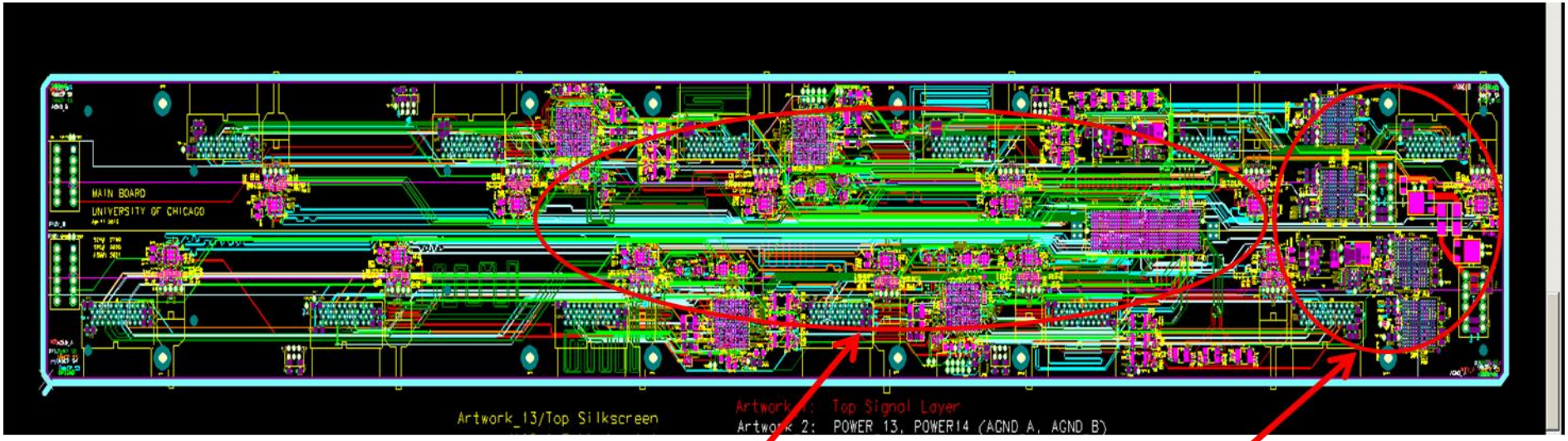




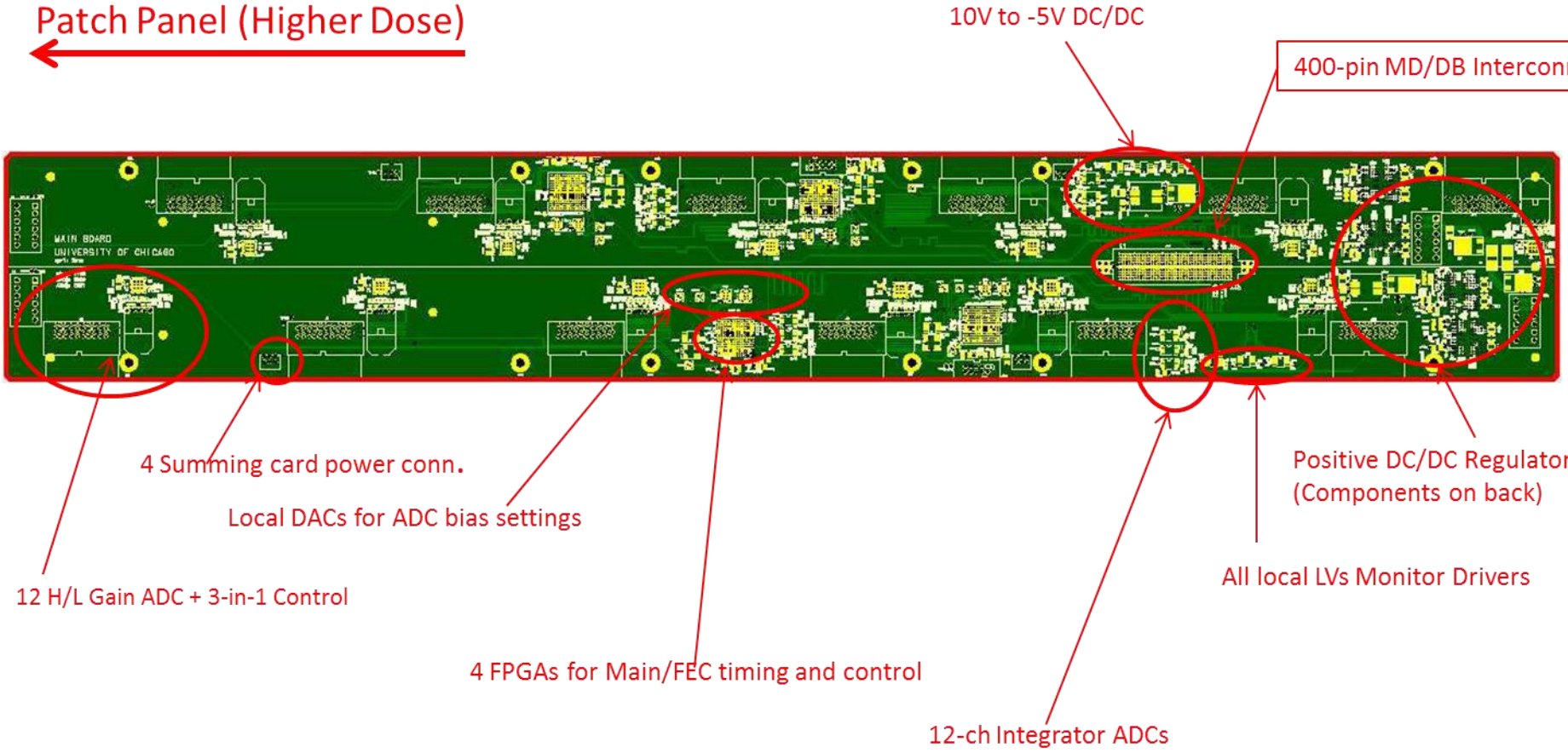
Main Board Design Considerations

- 6 signal layers, 8 power/ground layers
- 69 cm board length
- High speed: (560 Mbps)
- Max. trace length: 20 inches
- Crosstalk consideration
- Mixed signals (very low noise analog and very high speed digital)
- Equal timing route constraints
- Current rate constraints
- “Swish-cheese” effect on power planes (limit via usage)
- EMI and grounds loop isolations for DC/DC switchers





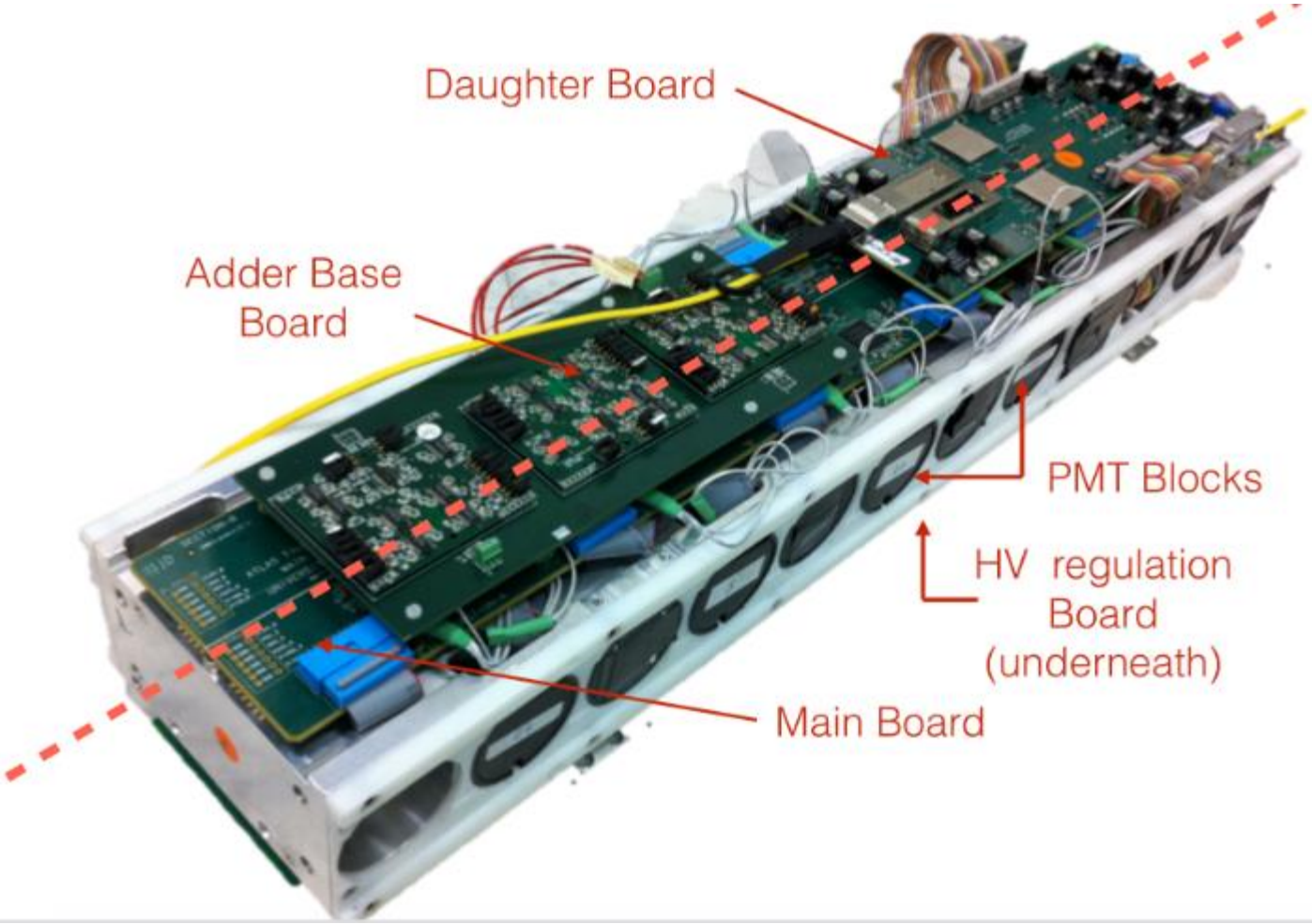
Component Placement



FEB Alternatives/Downselect

- The “3in1” Front-end board is the default, but we are looking at two ASIC alternatives that digitize on the FEB rather than on the MB
- If an ASIC FEB is chosen, the MB will not need ADCs
  - Cheaper MB
  - All the other functionality still needed
  - No significant impact on burn-in, testing and repair

R&D: Demonstrator Mini-drawer



Research and Development

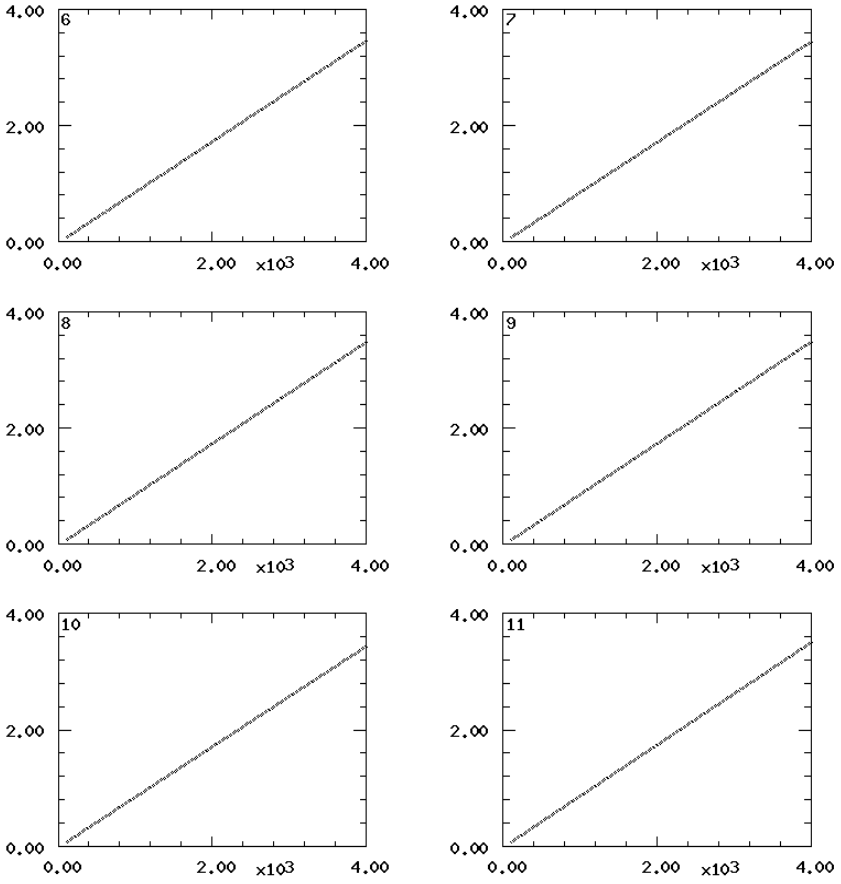
The Demonstrator Program

- R&D from USATLAS to build and evaluate demonstrators
  - 3in1, QIE front-end cards and Main Boards produced for demonstrator
  - LV, HV control boards designed and prototyped; LVboxes produced
  - Radiation certification of components and development of rad-hard optical modulator
- Good progress so far:
  - 2015: beam test of 3in1-based demonstrator (successful!)
  - 2016: two more beam tests to evaluate ASIC FEB's
  - 2016: simulations; which FEB handles pileup best?
  - 2017: experience with a demonstrator in ATLAS detector
  - 2017-2020: final integrated design, prototype, testing
    - Includes test beam running to measure Jet Energy Scale and radiation certification

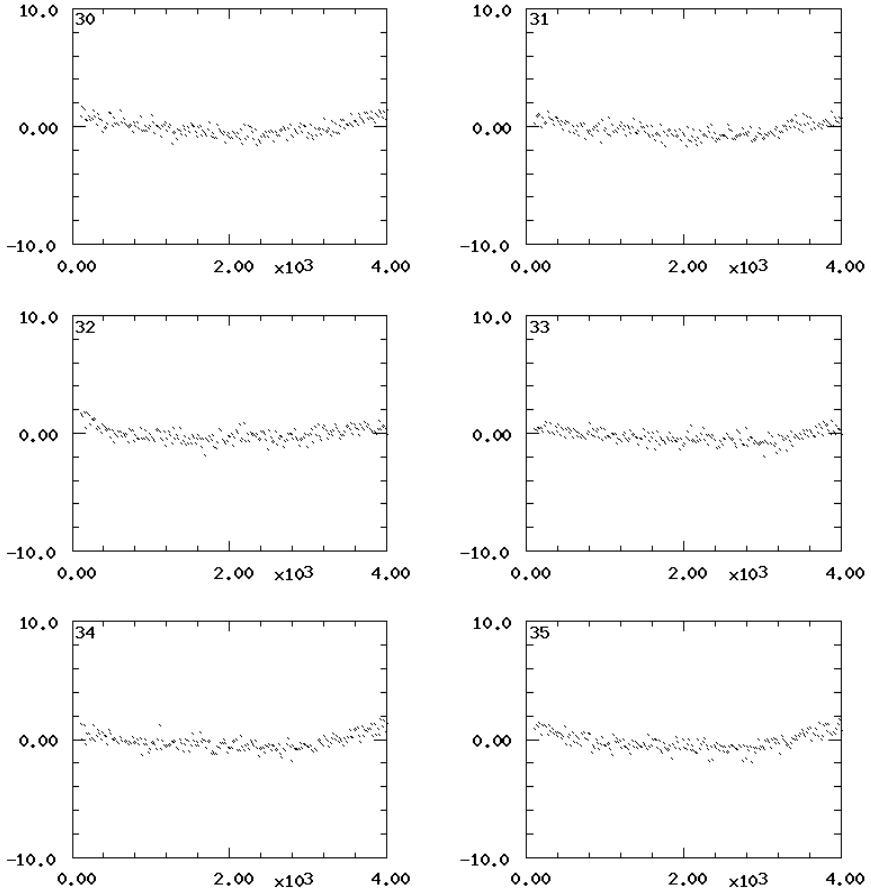
Excellent Performance Achieved

System linearity is excellent! Much better than 0.3% that present system required.

NL Plots (6-ch)



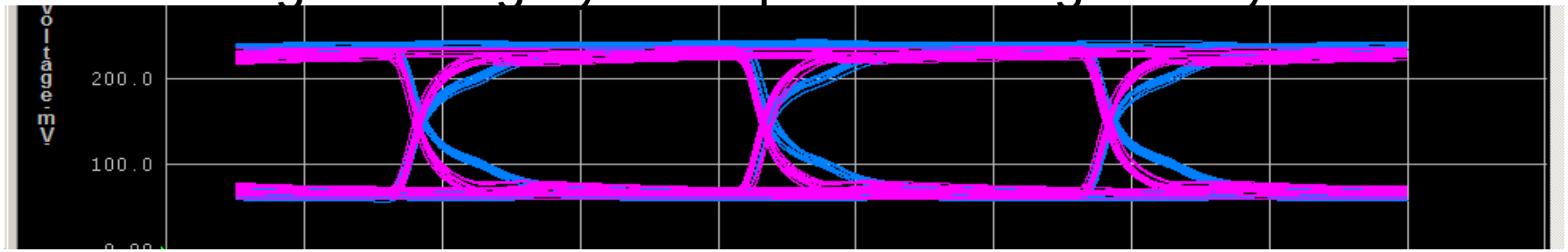
DNL over 12-bit ADC



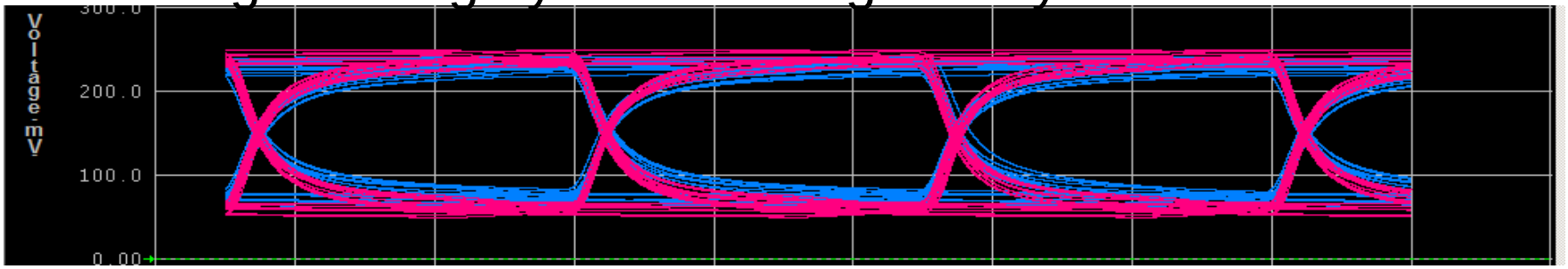
Performance: Low Noise

Diff. pairs: Top/Bottom layer, 20-inches (100-ohm)
Code: PRBS5 800Mbps (with 42% rate margin)

Signal Integrity on Top/Bottom Signal Layers



Signal Integrity on Inner Signal Layers



Costing Details: Components

- We have the Bill of Materials from prototype production
- We have quotes for PCB assembly in various lot sizes
- Propose to purchase all passive components in 1 lot (discount!)
  - More expensive IC's in two lots, assuming 20% conservative discount
- Summary of cost per Main Board (1100 needed; 100 preproduction):

Item:	Quantity of 100	Quantity of 550
Passive components	$96.23	$96.23
IC's	$704.38	$563.50
PCB	$400.00	$240.00
Assembly	$190.20	$182.00
total	$1,390.81	$1,081.73

Costing Details: Labor

- Parts packages, short-test PCB: 0.2 ET
- Oversee PCB assembly, initial testing, debugging with assy hse: 0.25 EE, 0.2 ET
- Mount in burn-in fixtures; supervise students: 0.4 EE, 1.2 ET, 1 Undergrad
- Diagnose and repair failures: 0.2 EE, 0.2 ET
- Inventory, crate and ship to CERN: 0.15
- Acceptance test training at CERN and system integration meetings: 0.4 EE

Summary: 1.25 EE, 1.95 ET, 2 Undergraduate Students for production phase.

Costing Table

WBS	Deliverable	Task	Labor Hrs	Labor $	M&S $	Travel $	Total $
6.5.1.1	**Main Boards**		**9,146**	**648,939**	**1,109,614**	**31,340**	**1,789,893**
	Production procurement	MB1120	355	27,982	883,850	0	911,832
	Engineers		0				
	Technicians		355				
	Student labor		0				
	Production PCB assembly	MB1130	710	73,183	200,200	500	273,883
	Engineers		355				
	Technicians		355				
	Student labor		0				
	Production Burn-in	MB1160	6,394	354,723	0	0	354,723
	Engineers		710				
	Technicians		2,131				
	Student labor		3,552				
	Production diagnose&repair	MB1170	710	75,379	0	0	75,379
	Engineers		355				
	Technicians		355				
	Student labor		0				
	Ship to CERN	MB1210	266	21,722	25,564	0	47,286
	Engineers		0				
	Technicians		266				
	Student labor		0				
	Acceptance test	MB1220	355	46,557	0	30,840	77,397
	Engineers		355				
	Technicians		0				
	Student labor		0				
	Management	MB1225	355	49,393	0	0	49,393
	Engineers		355				
	Technicians		0				
	Student labor		0				